

**REMARKS**

Applicant notes that this Amendment is filed concurrently with Appellant's Resubmission of Appeal Brief, and is substantially identical to the Amendment filed herein on January 21, 2004 and the Second Amendment filed on April 19, 2004.

Applicant notes that the Examiner telephoned Applicant's undersigned representative on May 7, 2004 and discussed the present Application with Applicant's undersigned representative. Applicant gratefully acknowledges the Examiner's indication to Applicant's undersigned counsel during this teleconference that the after-final Amendment filed on January 21, 2004 would indeed overcome the prior art of record, and, moreover, that the Examiner would not likely find any art in an updated search which would teach or suggest the claimed invention. The Examiner stated, however, that Applicant would have to file a Request for Continued Examination (RCE) before the Examiner would enter the Amendment.

However, as noted above, no new issue was raised by the Amendment filed on January 21, 2004. Indeed, the Amendment merely amends claims 29, 41 and 45-46 to replace the term "adjacent to" with "on", which was found in claim 57.

Moreover, the Examiner's remarks made during the above-referenced teleconference contradicts the Examiner's statement in the Advisory Action that "THE REPLY FILED FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE". That is, the Examiner indicated during the teleconference that the Amendment would place the Application in condition for allowance. Therefore, it was completely unreasonable for the Amendment not to be entered by the Examiner.

In summary, Applicant respectfully submits that the claim amendments included herein clearly do not raise new issues and serve to clarify the issues on appeal. Therefore, this Amendment should be entered.

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 29-39 and 41-57 are all the claims presently pending in the application. Claims 29, 41-42, 45-46 and 57 have been amended to more particularly define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 29-36, 41-42 and 45-57 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun (U.S. Patent No. 5,399,507). Claims 37-39 and 43-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sun, in further view of Tanaka (JP Patent No. 10-303385).

These rejections are respectfully traversed in the following discussion.

## I. THE CLAIMED INVENTION

The claimed invention (e.g., as recited in claim 29) is directed to a semiconductor device including a bulk silicon region comprising single crystal silicon, and a silicon-on-insulator (SOI) region which includes an insulator layer which is formed beneath an upper portion of the single crystal silicon and has at least one lateral end portion adjacent to a lower portion of the single crystal silicon, and at least one isolation oxide formed in the upper portion of the single crystal silicon so as to form at least one island of the single crystal silicon on an upper surface of the insulator layer. Importantly, the at least one isolation oxide includes a first isolation oxide formed adjacent to a first end portion of the insulator layer, a second isolation oxide formed adjacent to a second end portion of the insulator layer and **a third isolation oxide formed on a middle portion of the insulator layer**, the first and second isolation oxides extending laterally beyond the first and second end portions, respectively.

Conventional substrates having an SOI region are formed either by separation by implantation of oxygen (SIMOX) or by a cladding process where an oxide layer is formed in a first surface of a first substrate, a second substrate is bonded to the first surface, and elements are then formed in the second substrate. However, such conventional devices do not include a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation

oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively.

The claimed invention, on the other hand, includes a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively (Application at Figure 1C-1D; page 7, line 7-page 8, line 11).

In the claimed invention, the upper portion of silicon overlying the insulator layer may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and crystallizing the amorphous silicon by using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 17-21). However, in this case, non-ideal silicon may exist “on the seam where the crystallization of the epitaxial silicon from both edges meet” (Application at page 10, lines 7-12; Figure 1D). Thus, by forming an isolation oxide on a middle portion of the insulator layer, this “non-ideal” portion may be removed from the substrate (Application at page 10, lines 13-20).

## **II. THE PRIOR ART REFERENCES**

### **A. The Sun Reference**

The Examiner alleges that Sun teaches the claimed invention of claims 29-36, 41-42 and 45-57. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Sun.

Sun discloses a mixed thin-film and bulk semiconductor substrate (10, 30) for integrated circuit applications is made with two different processes. In the first process, a standard wafer (11) is masked around its periphery (14). The internal unmasked portion (16) is implanted with an insulating species to form a buried dielectric layer (18), thus forming a mixed thin-film and bulk semiconductor substrate. Alternatively, a thin-film wafer may be masked on an internal portion (36) and then etched to expose a portion (40) of the underlying bulk substrate (11')

around the periphery of the wafer. An epitaxial layer (50) is then grown to build up the exposed bulk portion to form the mixed substrate. An isolation region (24, 52, 46, 54) is formed at a boundary between the thin-film portion and the bulk portion. Devices (27, 28, 28') having different voltage requirements may then be formed overlying appropriate portions of the mixed substrate.

However, Sun does not teach or suggest “*wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively*”, as recited in claims 29, 41 and 45-46.

As noted above, unlike conventional substrates having an SOI region which are formed either by separation by implantation of oxygen (SIMOX) or by a cladding process, in the claimed invention, the upper portion of silicon overlying the insulator layer may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and crystallizing the amorphous silicon by using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 17-21). However, in this case, non-ideal silicon may exist “on the seam where the crystallization of the epitaxial silicon from both edges meet” (Application at page 10, lines 7-12; Figure 1D). Thus, by forming an isolation oxide on a middle portion of the insulator layer, this “non-ideal” portion may be removed from the substrate (Application at page 10, lines 13-20).

As a result, the claimed invention includes a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively (Application at Figure 1C-1D; page 7, line 7-page 8, line 11). This feature is not taught or suggested by conventional substrates.

Clearly, this feature is not taught or suggested by Sun. Indeed, the Examiner alleges that

this feature is disclosed in Sun at Figure 4 and col. 3, lines 34-38). However, this is clearly not correct.

Specifically, the Examiner attempts to equate the isolation region 22 in Sun, with the isolation oxide formed “on a middle portion” of the insulator layer in the claimed invention. However, Figure 4 does not show the isolation region 22 formed in the middle of the “buried dielectric layer” 18. Indeed, Figure 4 (as with the other drawings) cuts off the substrate 11, so it is impossible to determine at what portion of the dielectric layer 18 the isolation region 22 is formed.

In fact, nowhere does Sun teach or suggest forming the region 22 “on the middle portion” of the buried dielectric 18. Instead, Sun merely states that “[i]solation region 22 is formed solely in the thin-film portion 20 of the substrate 10” (Sun at col. 3, lines 28-29). Applicant points out that this could be many places other than “on the middle portion”. For example, this could be satisfied by forming the isolation region near the left edge of the dielectric layer 18, or near the right edge of the dielectric layer 18.

Moreover, Sun would have no reason to form the isolation region 22 in the middle portion of the buried dielectric 18. Indeed, the quality of the silicon above the dielectric 18 is the same over the length of the dielectric 18. Therefore, it would in no way benefit the Sun device to form the isolation region 22 in the middle of the dielectric. Thus, there would be no reason to modify the Sun device to include this feature.

Further, Sun is directed to a standard SIMOX process. As explained in the Application, SIMOX results in the silicon exposed to such implantation of oxygen having a large number of defects (in fact, this is one of the problems which the claimed invention is intended to address). Thus, the silicon regions above the dielectric layer 18 in Sun would contain a large amount of defects.

The claimed invention, on the other hand, does not result in defects being scattered all over the upper portion of the silicon substrate. Indeed, in the claimed invention, any defective portions may be localized (e.g., near a middle portion of the insulator layer) and can, therefore, be easily replaced with an isolation oxide.

In fact, these advantages of the claimed invention over a substrate subjected to a SIMOX process is clearly set forth in the Application. However, the Examiner somehow surprisingly refuses to recognize these benefits.

For example, the Examiner states in the Office Action that Sun does not teach that the silicon above the dielectric layer includes a defective region “in absence of evidence to the contrary” he considers the silicon islands to be substantially devoid of defects. **Applicant would respectfully point out that the specification states:**

*“as compared to the conventional patterned SIMOX technique, which results in a much higher number of defect counts per unit area (or defect density), the method of the present invention results in a much better substrate quality. This higher substrate quality is because the stress from lattice mismatch (e.g., of the oxide and the silicon) is more by high energy oxygen implantation. The defective regions resulting from the method of the present invention are also predictable and therefore can be completely removed in a subsequent shallow trench formation”* (Application at page.5, lines 2-10).

Thus, Applicant respectfully submits that there is plenty of evidence that the silicon above the dielectric layer in the Sun device includes a high number of defect counts per unit area. Indeed, this fact is extremely well known to any person of ordinary skill in this art. In fact, this is the only evidence in this case regarding the quality of the silicon above the dielectric layer. That is, there is no evidence in the case that would contradict the Application.

Further, with respect to claim 4, the Examiner states that it would obvious to modify Sun to include an angled sidewall of the insulator layer. However, Applicant would point out that it is impossible to form an angled sidewall using a SIMOX process as in Sun. Therefore, the Examiner is clearly incorrect.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Sun. Therefore, the Examiner is respectfully requested to withdraw this rejection.

**B. The Tanaka Reference**

The Examiner alleges that Tanaka would have been combined with Sun to form the claimed invention of claims 37-39 and 43-44. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Tanaka discloses a method of integrally forming a high-performance hybrid element. In the method, a silicon substrate 3 is exposed by selectively removing a silicon layer 1 and an insulating layer 2 from a silicon-on-insulator(SOI) substrate, and desired semiconductor elements 11 are respectively formed on the exposed silicon substrate 3 and the silicon layer 1 (Tanaka at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, Sun is directed to a method of forming a thin film and bulk semiconductor substrate using SIMOX, whereas Tanaka is directed to a method of forming a DRAM device. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the Examiner's allegations, neither of these references teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Sun, nor Tanaka, nor any combination thereof teaches or suggests *"wherein said at least one isolation oxide comprises a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first*

*and second end portions, respectively*”, as recited in claims 29, 41 and 45-46.

As noted above, unlike conventional substrates having an SOI region which are formed either by separation by implantation of oxygen (SIMOX) or by a cladding process, in the claimed invention, the upper portion of silicon overlying the insulator layer may be formed over the insulator layer by depositing amorphous silicon on the insulator layer and the lower portion of the single crystal silicon, and crystallizing the amorphous silicon by using the lower portion of the single crystal silicon as a crystal growth seed (Application at page 7, lines 17-21). However, in this case, non-ideal silicon may exist “on the seam where the crystallization of the epitaxial silicon from both edges meet” (Application at page 10, lines 7-12; Figure 1D). Thus, by forming an isolation oxide on a middle portion of the insulator layer, this “non-ideal” portion may be removed from the substrate (Application at page 10, lines 13-20).

Clearly, Tanaka does not teach or suggest these novel features. Indeed, the Examiner does not even rely on Tanaka as disclosing this feature, but only relies on Tanaka as allegedly disclosing a memory device formed in the bulk silicon region and a logic device formed in said SOI region.

In fact, Tanaka merely discloses that a logic circuit 13 is formed on silicon layer 1, and a memory cell 11 is formed on the substrate 3 (Tanaka at Figure 1(f)). However, the silicon layer 1 is formed above the silicon substrate 3, which is completely different from the claimed invention. Thus, nowhere does Tanaka teach or suggest a first isolation oxide formed adjacent to a first end portion of said insulator layer, a second isolation oxide formed adjacent to a second end portion of said insulator layer and a third isolation oxide formed on a middle portion of said insulator layer, said first and second isolation oxides extending laterally beyond said first and second end portions, respectively. Therefore, Tanaka does not make up for the deficiencies of Sun.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.



### III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 29-39 and 41-57, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: \_\_\_\_\_

01/14/04



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